In the Claims:

1. (Original) A content addressable memory (CAM) device, comprising:

a priority resolution circuit that is configured to hierarchically resolve competing soft priorities between a plurality of active hit signals according to numeric significance.

2. (Original) The CAM device of Claim 1, wherein said priority resolution circuit is configured to resolve competing hard priorities between two or more of the plurality of active hit signals having equivalent highest soft priorities by identifying which of the two or more of the plurality of active hits signals has the highest hard priority.

3. (Original) The CAM device of Claim 2, wherein said priority resolution circuit comprises a MSB soft priority resolution stage and a LSB soft priority resolution stage.

4. (Original) The CAM device of Claim 3, wherein said priority resolution circuit comprises a hard priority resolution stage that is electrically coupled to outputs of said LSB soft priority resolution stage.

5. (Original) The CAM device of Claim 1, further comprising:

a plurality of CAM array blocks having respective soft priorities assigned thereto; and

wherein said priority resolution circuit comprises a plurality of registers that retain the soft priorities assigned to said plurality of CAM array blocks.

6. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks having respective soft priorities assigned thereto; and

a hierarchical priority resolution circuit that is configured to identify a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by ~~sequentially~~ evaluating the soft priorities of said plurality of CAM array blocks according to numeric significance.

7. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit is configured to sequentially evaluate the soft priorities of said plurality of CAM array blocks in descending order according to numeric significance.

8. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises a plurality of programmable registers that retain the soft priorities.

9. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises:

a first soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines; and

a second soft priority resolution circuit that is electrically coupled in a wired-OR manner to a second plurality of signal lines.

10. (Original) The CAM device of Claim 9, wherein the first and second plurality of signal lines are floated or biased at precharged levels during the search operation.

11. (Original) The CAM device of Claim 9, wherein said hierarchical priority resolution circuit further comprises:

a third soft priority resolution circuit that is electrically coupled in a wired-OR manner to a third plurality of signal lines.

12. (Original) The CAM device of Claim 11, wherein said hierarchical priority resolution circuit further comprises:

a hard priority resolution circuit that is electrically coupled to outputs of said third soft priority resolution circuit.

13. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises:

a soft priority resolution circuit; and

a hard priority resolution circuit that is electrically coupled to outputs of said soft priority resolution circuit.

14. (Original) The CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises:

a soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines that are floated or biased at precharged levels during a priority resolution operation; and

a hard priority resolution circuit that is electrically coupled to outputs of said soft priority resolution circuit.

15. (Original) A content addressable memory (CAM) device, comprising:

a priority resolution circuit that is configured to resolve competing soft priorities between a plurality of active hit signals associated with a respective plurality of CAM array blocks, in response to a search operation.

16. (Original) The CAM device of Claim 15, wherein said priority resolution circuit is configured to resolve competing hard priorities between at least two of the active hit signals having the same soft priority.

17. (Original) The CAM device of Claim 16, wherein said priority resolution circuit is a hierarchical priority resolution circuit having at least a MSB soft priority resolution stage and a LSB soft priority resolution stage.

18. (Original) The CAM device of Claim 17, wherein said priority resolution circuit comprises a hard priority resolution stage that is electrically coupled to outputs of said LSB soft priority resolution stage.

19. (Original) A content addressable memory (CAM) device, comprising:

a priority resolution circuit that is configured to resolve competing soft priorities between a plurality of active hit signals associated with a corresponding plurality of CAM array blocks in order to identify two or more active hit signals having highest equivalent soft priorities and is further configured to resolve competing hard priorities between the two or more active hit signals in order to identify one as having the highest hard priority.

20. (Original) The CAM device of Claim 19, wherein the competing soft priorities of the plurality of active hit signals are resolved by evaluating the soft priorities in a MSB to LSB sequence.

21. (Original) The CAM device of Claim 19, wherein said priority resolution circuit is a hierarchical priority resolution circuit having at least two soft priority resolution stages and a hard priority resolution stage.

22. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks having respective soft priorities assigned thereto; and

means for identifying a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by ~~sequentially~~ evaluating the soft priorities of said plurality of CAM array blocks according to numeric significance.

23. (Currently amended) A content addressable memory (CAM) device, comprising:

a hierarchical priority resolution circuit that is configured to identify a highest priority one of a plurality of CAM array blocks having respective matching entries therein during a search operation by ~~sequentially~~ evaluating soft priorities of the plurality of CAM array blocks according to numeric significance and evaluating competing hard priorities between at least two of the plurality of CAM array blocks having the same soft priorities.

24. (Original) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that each have respective soft and hard priorities assigned thereto; and

a priority resolution circuit that is configured to identify a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation by resolving competing hard priorities between at least two of said plurality of CAM array blocks having the same soft priority.

25. (Original) The CAM device of Claim 24, wherein the CAM device comprises 2^{N+1} CAM array blocks therein, where N is an integer; and wherein said priority resolution circuit comprises $\log_2 N$ groups of precharged signal lines that are used during a priority resolution operation to resolve competing soft priorities between hit signals generated by said plurality of CAM array blocks.

26. (Original) The CAM device of Claim 24, wherein the CAM device comprises 2^{N+1} CAM array blocks, where N is an integer; and wherein said priority resolution circuit comprises $\log_2 N$ groups of N or N-1 precharged signal lines.

27. (Original) The CAM device of Claim 24, wherein the CAM device comprises $(2^x)^y$ CAM array blocks, where x and y are integers; and wherein said priority resolution circuit comprises y groups of precharged signal lines having 2^x or 2^x-1 signal lines per group.

28. (Original) The CAM device of Claim 27, wherein x and y represent a pair of integers selected from the pair groups (x,y) consisting of (3,3), (2,4) and (3,2).

29. (Currently amended) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that each have respective soft and hard priorities associated therewith; and

means for identifying a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by ~~sequentially~~ resolving competing soft priories between said plurality of CAM array blocks and then resolving competing hard priorities between at least two of said plurality of CAM array blocks having equal soft priorities.

30. (Original) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that each have respective soft priorities associated therewith that are programmable and respective hard priorities associated therewith that are fixed according to layout position; and

a soft priority resolution circuit that is configured to process first and second active hit signals generated by first and second CAM array blocks within said plurality of CAM array blocks during a search operation, respectively, using wired-OR logic to identify a highest priority one of the first and second active hit signals and selectively block another one of the first and second active hit signals from being further processed as a highest priority candidate.

31. (Original) A content addressable memory (CAM) device, comprising:

a soft priority resolution circuit that is electrically connected in a wired-OR manner to a plurality of hierarchical control signal lines.

32. (Original) A content addressable memory (CAM) device, comprising:

a soft priority resolution circuit that is configured to resolve an active input hit signal as an active or inactive output hit signal by comparing a value of a plurality of soft priority input signals, which identify a soft priority of the active input hit signal, against a value of a plurality of hierarchical control signals.

33. (Original) A content addressable memory (CAM) device, comprising:

a first soft priority resolution circuit that is configured to resolve a first active hit signal as an active or inactive first output hit signal by comparing a value of a plurality of first soft priority input signals associated with the first active hit signal against a value of a plurality of hierarchical control signals; and

a second soft priority resolution circuit that is configured to resolve a second active hit signal as an active or inactive second output hit signal by comparing a value of a plurality of second soft priority input signals associated with the second active hit signal against the value of the plurality of hierarchical control signals.

34. (Original) A method of operating a content addressable memory (CAM) device, comprising the steps of:

applying a comparand to a plurality of CAM array blocks during a search operation to thereby detect a plurality of matching entries in the plurality of CAM array blocks;

generating, in response to the search operation, a plurality of active hit signals having respective soft and hard priorities associated therewith that correspond to soft and hard priorities of respective ones of the plurality of CAM array blocks;

resolving competing soft priorities between the plurality of active hit signals; and

resolving competing hard priorities between at least two of the active hit signals having equal soft priorities.

35. (Original) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that generate respective hit signals in response to a search operation;

a soft priority resolution circuit that is responsive to the hit signals and resolves competing soft priorities therebetween; and

a hard priority resolution circuit that resolves competing hard priorities between at least two output hit signals of equivalent soft priority generated by said soft priority resolution circuit.

36. (Original) A content addressable memory (CAM) device, comprising:

a segment of N CAM array blocks, where N is an integer; and

a soft priority resolution circuit that is responsive to hit signals generated by said segment and comprises N columns of soft priority resolution circuitry that are electrically coupled in a wired-OR manner to a plurality of hierarchical control signal lines.

37. (Original) The CAM device of Claim 36, further comprising:

a hard priority resolution circuit electrically coupled to outputs of said soft priority resolution circuit.

38. (Original) A method of resolving competing priorities between a plurality of active hit signals generated in a content addressable memory (CAM) device, comprising the step of:

passing the active hit signals through a soft priority resolution circuit that causes the active hit signals to compete against each other according to their respective soft priority values.

39. (Original) The method of Claim 38, wherein said passing step is followed by the step of passing all active hit signals that win the competition in the soft priority resolution circuit to a hard priority resolution circuit that selects the winning active hit signal having the highest hard priority associated therewith.

40. (Original) The method of Claim 38, wherein the soft priority resolution circuit causes the active hit signals to compete against each other in an MSB to LSB sequence according to their respective soft priority values.

Claims 41-45 (Canceled).

46. (Original) A content addressable memory (CAM) device, comprising:

$(2^x)^y$ CAM array blocks; and

a soft priority resolution circuit that hierarchically resolves competing soft priorities between a plurality of active hit signals generated a plurality of the CAM array blocks and comprises y groups of precharged signal lines having 2^x or 2^x-1 signal lines per group.

47. (Original) The CAM device of Claim 46, wherein x and y represent a pair of integers selected from the pair groups (x,y) consisting of (3,3), (2,4) and (3,2).

48. (Original) An integrated circuit device, comprising:

a plurality of CAM array blocks that are configured to generate respective hit signals in response to a search operation; and

encoding logic that is configured to identify an active one of the hit signals as having a highest soft priority from the hit signals generated by said plurality of CAM array blocks.

49. (Original) The device of Claim 48, wherein said encoding logic comprises:

a cross-point switch having data inputs that receive the hit signals generated by said plurality of CAM array blocks; and

a priority encoder having inputs that are electrically coupled to outputs of said cross-point switch.

50. (Original) The device of Claim 49, wherein said encoding logic further comprises a programmable register that retains addresses of said plurality of CAM array blocks; and wherein outputs of said programmable register are electrically coupled to select inputs of said cross-point switch.

51. (Original) An integrated circuit device, comprising:

a plurality of CAM array blocks that are configured to generate respective hit signals and respective index signals in response to a search operation; and

encoding logic that is configured to identify an active one of the hit signals having a highest soft priority from the hit signals generated by said plurality of CAM array blocks and is further configured to select an index signal associated with a CAM array block that generated the active one of the hit signals having a highest soft priority.

52. (Original) The device of Claim 51, wherein the index signal is a row address of a matching entry within the CAM array block that generated the active one of the hit signals having a highest soft priority.

53. (Original) The device of Claim 52, wherein said encoding logic is further configured to generate an output index signal that comprises a block address of the CAM array block that generated the active one of the hit signals having a highest soft priority.

54. (Original) The device of Claim 52, wherein said encoding logic comprises:

a cross-point switch having data inputs that receive the hit signals generated by said plurality of CAM array blocks; and

a priority encoder having inputs that are electrically coupled to outputs of said cross-point switch.

55. (Original) The device of Claim 54, wherein said encoding logic further comprises a programmable register that retains block addresses of said plurality of CAM array blocks as routing values; and wherein outputs of said programmable register are electrically coupled to select inputs of said cross-point switch.

56. (Original) An integrated circuit device, comprising:

a plurality of CAM array blocks that are configured to generate respective hit signals in response to a search operation; and

means for identifying an active one of the hit signals as having a highest soft priority from the hit signals generated by said plurality of CAM array blocks.

57. (Original) A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks that are configured to respond to a search operation by generating active hit signals having different soft priorities; and

means for generating a row address of a matching entry in an identified one of said plurality of CAM array blocks that generated an active hit signal having a highest soft priority.

58. (New) A content addressable memory (CAM) system, comprising:

a plurality of CAM array blocks having respective soft priorities assigned thereto; and

encoding logic responsive to a plurality of active hit signals generated by said plurality of CAM array blocks during a search operation, said encoding logic configured to resolve competing priorities between the plurality of active hit signals using programmable routing values assigned to the plurality of active hit signals.